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A Concurrent Multi-threaded Core for Complex SoCs

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Contributors

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Outline

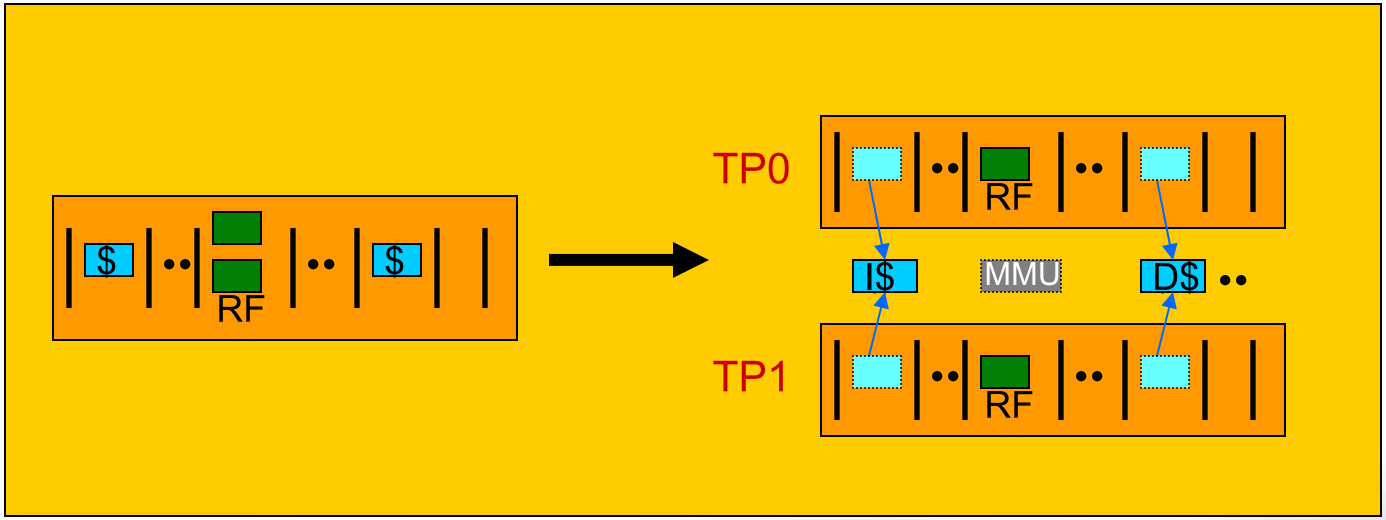
- Concurrent multi-threaded (CMT) cores
- CMT at the processor level
- CMT at the system level
- Performance
- Summary

Background

- Requirements of complex SoC applications
  - Predictable performance for control processors and application processors
  - Some degree of data sharing between the processors
- Approach
  - Start with multi-threading for low cost and low power
  - Avoid the cost of SMP or multi-cores
  - Based on existing MIPS32™ processor core

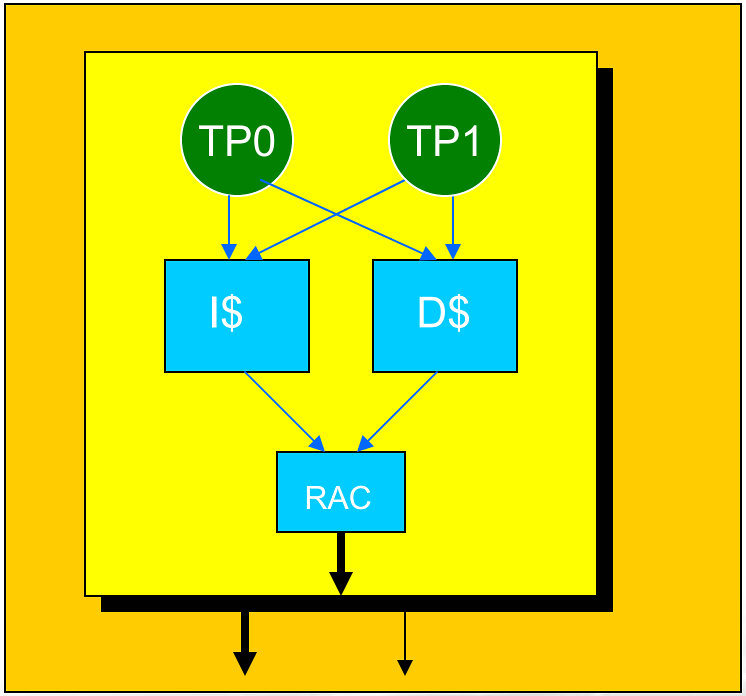
CMT- Concurrent Multi-Threading

- Multiple execution elements - thread processor (TP)
  - Each TP: Integer pipeline (w/ALU) and Register file
- Share the rest of resources
  - Caches, memory hierarchy, system interface
- System dependent - partitioned or shared
  - Memory management unit (TLB), application specific elements, EJTAG, etc.



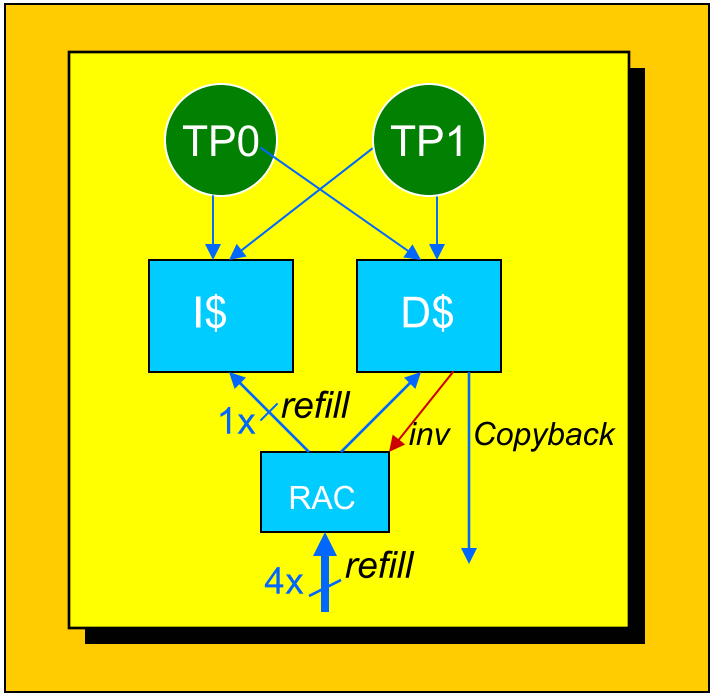
Balanced System Performance

- Performance improvement at the processors and memory must be in sync
- Non-blocking memory paths - all types of memory accesses
- Separate memory bus and system bus
- Readahead Cache (RAC) as a level-two cache

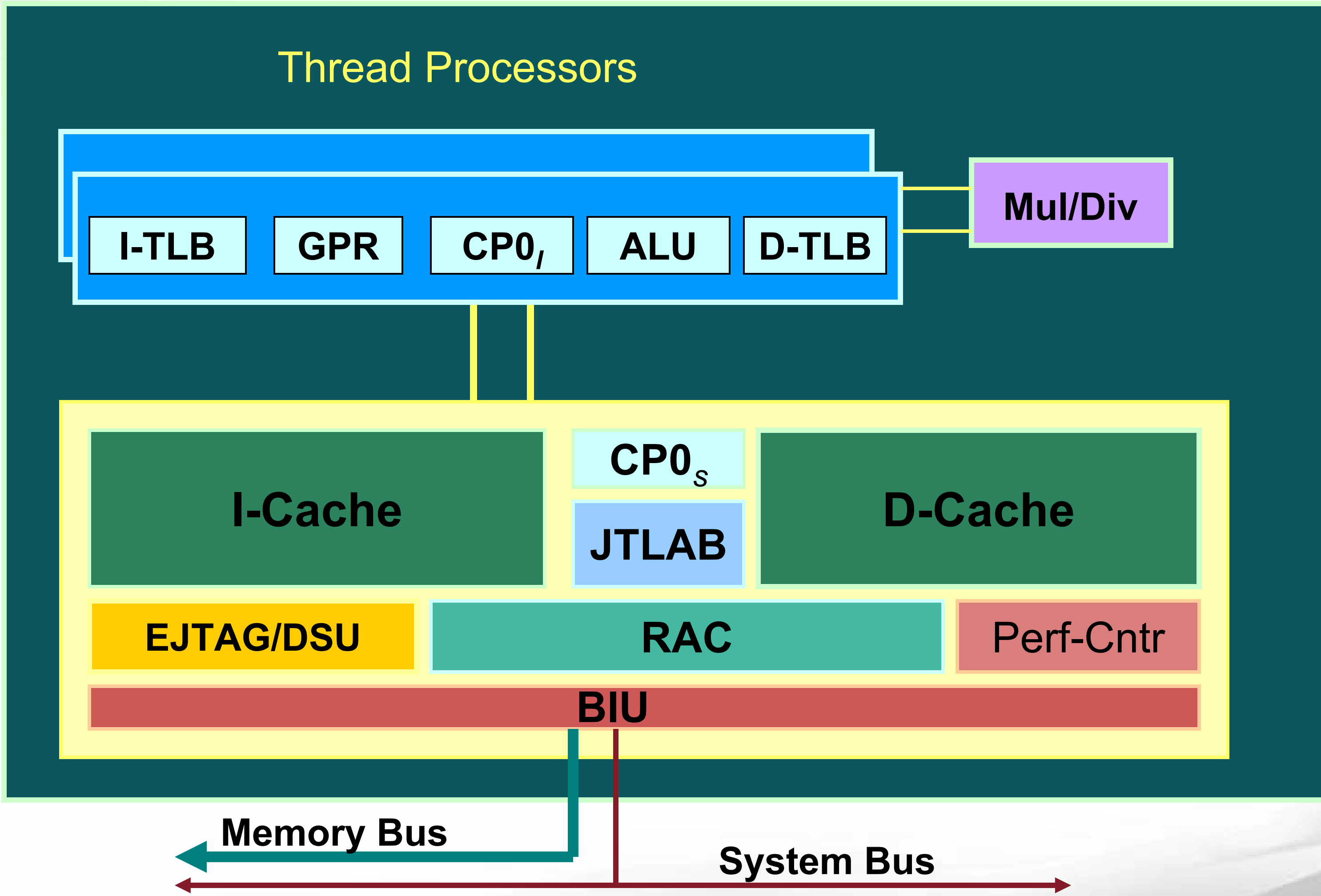


RAC- Readahead Cache

- Partial L2 Cache mainly for spatial locality
  - Large lines (at least 4x) but tiny capacity
- Supports next-line (NL) prefetching
- Supports PREFETCH instruction
- Transparent to the application
  - CACHE invalidate instruction
- Programmable per TP
  - use-I, use-D, NL-prefetch-I, NL-prefetch-D,
  - Invalidate, CACHE invalidate

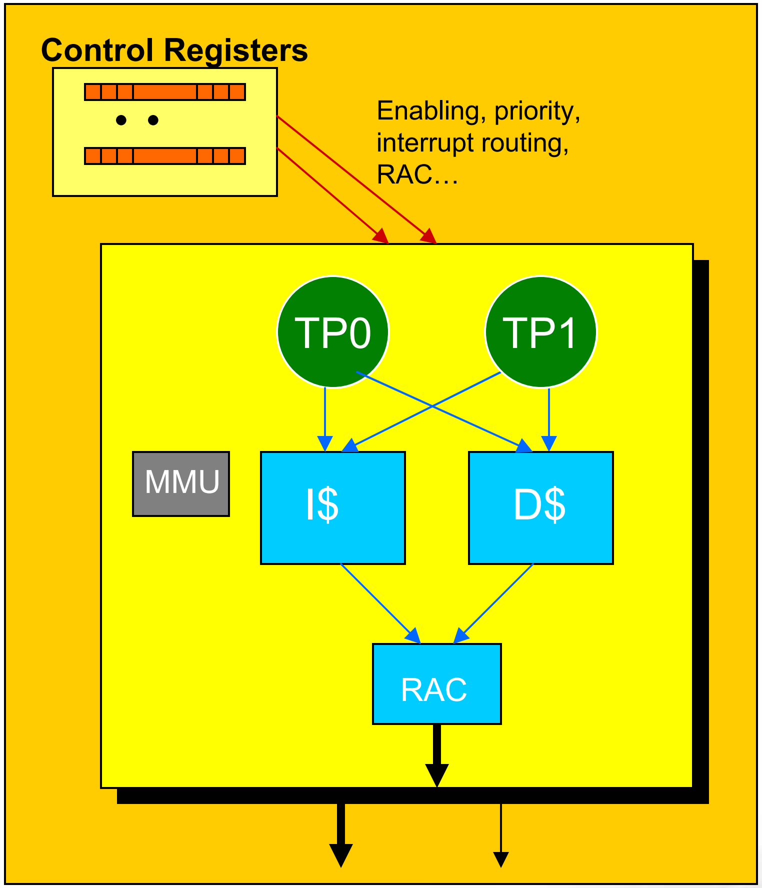


CMT Block Diagram



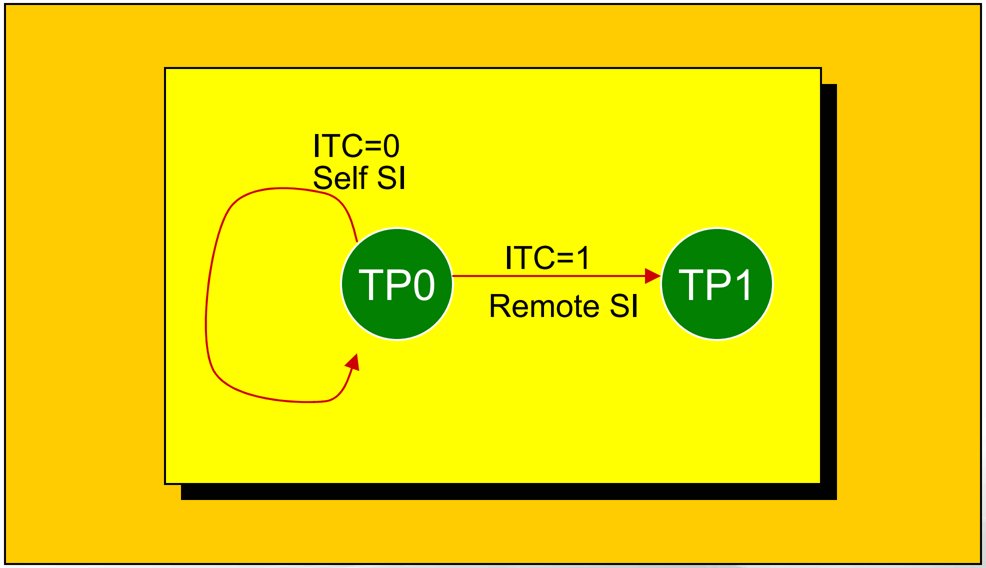
CMT Control

- Programmed through the control registers
- TP enabling & exception handling
  - TP0 enables TP1
  - Each TP can handle any execution exception
- Priority at the shared resources
  - A priority for concurrent accesses at a resource
  - i) Fair (random then FIFO), ii) high-priority TP
- External interrupts
  - Each external interrupt can be routed to a TP
- Other functions
  - RAC, inter-TP communication, etc.



CMT Communication

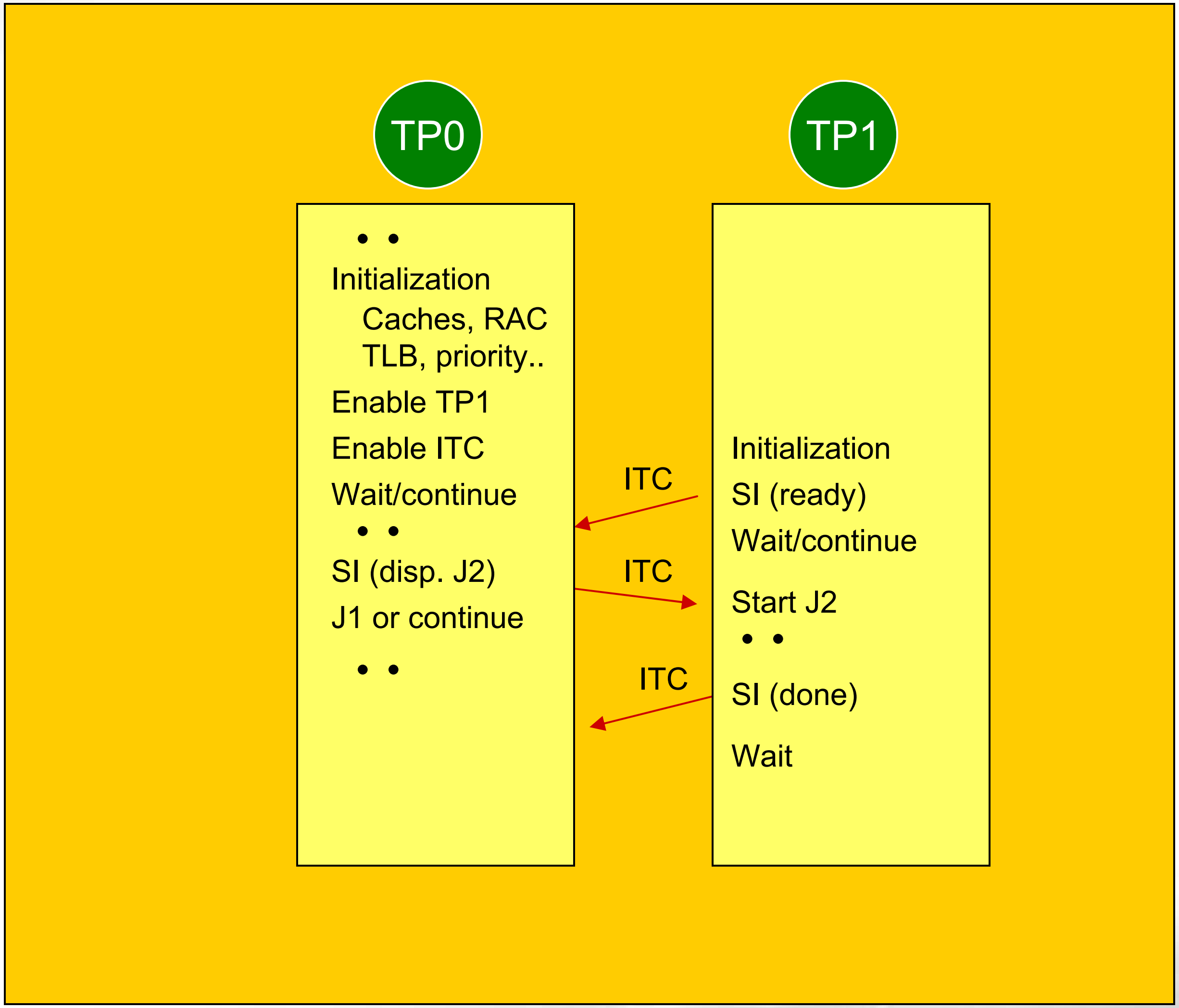
- Shared memory multiprocessing
  - Data coherency automatically achieved through the shared data cache
  - Atomic operations: LL (load link) and SC (Store Conditional)
- Inter-thread communication (ITC)
  - Through the software interrupt (SI)
  - After ITC in the control register is enabled, a TP writing to an SI bit triggers an SI at the remote TP



Special SoC Support

- Predictable performance for certain tasks
  - Set priority of shared resources
  - Partition of cache space
  - Stop the low priority TP
- Exception serialization
  - Serialization mechanism to allow one exception (from one of the TPs) at a time
  - Shared TLB: serialized simultaneous TLB exceptions

A Programming Example



Performance

- Dhrystone 2.1: Benchmark measures core performance
- Each TP runs a copy of Dhrystone
  - Performance of 6-stage pipeline at 1 TP: 1.5 DMIPS/MHz, w/GreenHills 4.0
  - Averaged CMT performance- 1.8x
  - Total DMIPS = 1.5 DMIPS/MHz x 1.8 @ 300 MHz, or 810 DMIPS

➢ Higher performance (throughput) than a single core of 500 MHz

Summary

- Tightly-coupled multiprocessing suitable for complex embedded applications
  - On-core control of load balance and performance assurance
  - Single-system image
- Effective cost and performance trade-off
  - Cost close to that of multi-threaded processors while performance close to that of symmetrical multiprocessors (SMP)
- Allows systems to increase processor performance without major re-design